Interference Print Out

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1	BRS	L1	643	(dynamic adj simulation)	US-PGPUB; USPAT; EPO; JPO	2005/12/16 14:50
2	BRS	L2	31	(dynamic adj simulation)	EPO; JPO	2005/12/16 14:46
3	BRS	L3	2	(dynamic adj simulation) and timing	EPO; JPO	2005/12/16 14:46
4	BRS	L4	0	(dynamic adj simulation) and timing and skip	EPO; JPO	2005/12/16 14:46
5	BRS	L6	22	(dynamic adj simulation).clm.	US-PGPUB	2005/12/16 14:49
6	BRS	L7	2	(dynamic adj simulation).clm. and netlist.clm.	US-PGPUB	2005/12/16 14:50
7	BRS	L11	2	(dynamic adj timing adj simulation)	US-PGPUB	2005/12/16 14:55
8	BRS	L12	0	(dynamic adj timing adj simulation).clm.	US-PGPUB	2005/12/16 14:55
9	BRS	L13	0	(netlist).clm. same (maximum adj forward adj delay).clm.	US-PGPUB	2005/12/16 14:55
10	BRS	L14	0	(netlist).clm. and (maximum adj forward adj delay).clm.	US-PGPUB	2005/12/16 14:56
11	BRS	L15	35	(timing same checks).clm.	US-PGPUB	2005/12/16 14:56
12	BRS	L16	0	(timing same checks).clm. and (simulation).clm.	US-PGPUB	2005/12/16 14:56
13	BRS	L17	4	(timing same checks).clm. and (simulation).clm.	US-PGPUB	2005/12/16 14:56

TS

	Type	Ref #	Hits	Search Text
1	BRS	S1	0	(multi adj packet) same label
2	BRS	S2	169	multi same packet same label
3	BRS	S3	143	multi same packet same label same switching
4	BRS	S4	31	multi same packet same label same switching same protocols
5	BRS	S5	17	(multi same packet same label same switching same protocols) and egress
6	BRS	S6	73	(multi same packet same label same switching same protocols) and egress
7	BRS	S7	61	(multi same packet same label same switching same protocols) and egress and header
8	BRS	S8	61	(multi same packet same label same switching same protocols) and egress and header and packets
9	BRS	S9	61	(multi same packet same label same switching same protocols) and egress and header$ and packets
10	BRS	S10	11	(multi same packet same label same switching same protocols) and egress and header$ and packets and emulation
11	BRS	S11	0	(circuit same emulation) and (protocols same header$) and datastream and egress
12	BRS	S12	25	(circuit same emulation) and (protocols same header$) and (data adj stream) and egress
13	BRS	S13	0	(circuit same emulation) and (protocols same header$) and (data adj stream) and egress and MPLS
14	BRS	S14	19	(circuit same emulation) and MPLS
15	BRS	S15	4	(circuit same emulation) and MPLS and valid$
16	BRS	S16	2	(circuit same emulation) and multi-packet
17	BRS	S17	0	703/26.ccls. and (protocols same header$) and (data adj stream) and egress
18	BRS	S18	0	703/26.ccls. and (data adj stream) and egress
19	BRS	S19	1	703/26.ccls. and egress
20	BRS	S20	38	filter adj resource
21	BRS	S21	0	filter adj resource adj estim$
22	BRS	S22	0	filter adj resource adj estimator
23	BRS	S23	38	filter adj resource
24	BRS	S24	4	(dynamic adj timing adj simulation)
25	BRS	S25	4	(dynamic adj timing adj simulation) and delays
26	BRS	S26	0	(dynamic adj timing adj simulation) and delays and safe
27	BRS	S27	0	(dynamic adj timing adj simulation) and (delays near safe)
28	BRS	S28	0	(dynamic adj timing adj simulation) and safe
29	BRS	S29	0	(dynamic adj timing adj simulation) and reverse
30	BRS	S30	37210	(logic same delays)
31	BRS	S31	13	(logic same delays) and (safe adj delays)
32	BRS	S32	0	(logic same delays) and (safe adj delays) and reverse and sum
33	BRS	S33	5	(logic same delays) and (safe adj delays) and reverse
34	BRS	S34	23	713/500.ccls. and safe
35	BRS	S35	4	713/500.ccls. and safe and checks and reverse
36	BRS	S36	0	713/500.ccls. and (mimum near reverse)
37	BRS	S37	3	713/500.ccls. and safe and checks and reverse and simulation
38	BRS	S38	3	713/500.ccls. and safe and checks and reverse and simulation and remove

	Type	Ref #	Hits	Search Text
80	BRS	S81	0	((dynamic adj simulation) same logic) and sequential and netlist and delay and (netlist same simulation) and (skip$) and (maximum near delay)
81	BRS	S80	1	((dynamic adj simulation) same logic) and sequential and netlist and delay and (netlist same simulation) and (skip$) and (maximum)
82	BRS	S82	181	703/19.ccls.
83	BRS	S83	52	703/19.ccls. and dynamic
84	BRS	S84	1	703/19.ccls. and (dynamic adj simulation)
85	BRS	S85	0	703/19.ccls. and (dynamic adj simulation) and nodes and delays
86	BRS	S86	1	"6300891".pn.
87	BRS	S87	0	"6300891".pn. and timing
88	BRS	S88	379	(dynamic adj simulation)
89	BRS	S89	0	(dynamic adj simulation) and (delay same summary)
90	BRS	S90	8	(dynamic adj simulation) and (delay same netlist)
91	BRS	S91	6	(dynamic adj simulation) and (delay same netlist) and sequential
92	BRS	S92	6	(dynamic adj simulation) and (delay same netlist) and sequential and timing
93	BRS	S93	0	(dynamic adj simulation) and (delay same netlist) and sequential and timing and skip
94	BRS	S94	6	(dynamic adj simulation) and (delay same netlist) and sequential and timing and zero
95	BRS	S95	5	(dynamic adj simulation) and (delay same netlist) and sequential and timing and (zero adj delay)
96	BRS	S96	5	(dynamic adj simulation) and (delay same netlist) and sequential and timing and (zero adj delay) and performance
97	BRS	S97	5	(dynamic adj simulation) and (delay same netlist) and sequential and timing and (zero adj delay) and performance and nodes
98	BRS	S99	0	(dynamic adj simulation) and (delay same netlist) and sequential and timing and (zero adj delay) and performance and nodes and (remove near time)
99	BRS	S100	0	(dynamic adj simulation) and (delay same netlist) and sequential and timing and (zero adj delay) and performance and nodes and (remove near timing)
100	BRS	S98	5	(dynamic adj simulation) and (delay same netlist) and sequential and timing and (zero adj delay) and performance and nodes and remove

	Type	L #	Hits	Search Text	DBs	Time Stamp
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2	BRS	L2	31	(dynamic adj simulation)	EPO; JPO	2005/12/16 14:46
3	BRS	L3	2	(dynamic adj simulation) and timing	EPO; JPO	2005/12/16 14:46
4	BRS	L4	0	(dynamic adj simulation) and timing and skip	EPO; JPO	2005/12/16 14:46

39	BRS	S39	3	713/500.ccls. and safe and checks and reverse and simulation and (remove near/2 check)

	Type	Ref #	Hits	Search Text
80	BRS	S81	0	((dynamic adj simulation) same logic) and sequential and netlist and delay and (netlist same simulation) and (skip$) and (maximum near delay)
81	BRS	S80	1	((dynamic adj simulation) same logic) and sequential and netlist and delay and (netlist same simulation) and (skip$) and (maximum)

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	181	703/19.ccls.	USPAT	2005/12/16 13:02
2	BRS	L2	52	703/19.ccls. and dynamic	USPAT	2005/12/16 13:02
3	BRS	L3	1	703/19.ccls. and (dynamic adj simulation)	USPAT	2005/12/16 13:03
4	BRS	L4	0	703/19.ccls. and (dynamic adj simulation) and nodes and delays	USPAT	2005/12/16 13:03

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A Johnsson, M Bjoerkman, B Melander - Proceedings of the International Conference on Communication ... - idt.mdh.se
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Bandwidth Measurements in Wired and Wireless Networks
A Johnsson, S Vasteras - mrtc.mdh.se
... and Mats Bjorkman, In proceedings to the International Conference on Communication in Computing, Special Session on Net- work **Simulation** and Performance ...
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Performance Evaluation of an End-to-End Measurement Based Call Admission Control Method
B Soos - axelero.hu
... 3.7.2. A Sample **Simulation**.....37 ... the sampling techniques, **timing**, frequency, scheduling ...
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Probing-Based Approaches to Bandwidth Measurements and Network Path Emulation
B Melander - user.it.uu.se
... 2000 Paper D: c **Simulation** Councils, Inc. 2002 vii ... performed all of the experiments and done most of the analysis of the measurement and **simulation** data. ...
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Estimating available bandwidth using packet pair probing
N Hu, PA Steenkiste - 2002 - dcs.st-andrews.ac.uk
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[PS] Study of a non intrusive and accurate method for measuring the end-to-end useful bandwidth
M Goutelle, P Primet, IR LIP - ens-lyon.fr
... available bandwidth. This method has been validated in **simulation**, then implemented in Linux and validated experimentally. We compare ...
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JR Albrecht - strength.ucsd.edu
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A Collins - cs.washington.edu
... For **simulation** we would likely prefer a more realistic model, even at the ... most true endpoint techniques, the data consist of packet **timing** information, which ...
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Active Probing using Packet Quartets
A Pisztor, D Veitch - portal.acm.org
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... pdfs of cell/interconnect **delays** Cell-based **netlist** ... from critical **nodes** such that all **nodes** on the ... cell/interconnect **delays** cell/interconnect **delays** with a ...
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J Ferguson - System-on-Chip for Real-Time Applications, 2003. Proceedings ... - ieeexplore.ieee.org
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[PS] Rapid Prototyping of IP Blocks in SoC Designs
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... 61 7.3.2 **Dynamic Timing Simulation** . ... has lead to a situa- tion where the most remarkable **delays** inside the ... cores, is that a rm IP core is as a **netlist**, but it ...
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Rim, M.; Jain, R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 13, Issue 4, April 1994 Page(s):451 - 458
Digital Object Identifier 10.1109/43.275355
AbstractPlus | Full Text: PDF(668 KB) **IEEE JNL**

2. **A fault-tolerant array processor designed for testability and self-reconfigu**
Jain, A.; Mandava, B.; Rajski, J.; Rumin, N.C.;
Solid-State Circuits, IEEE Journal of
Volume 26, Issue 5, May 1991 Page(s):778 - 788
Digital Object Identifier 10.1109/4.78249
AbstractPlus | Full Text: PDF(968 KB) **IEEE JNL**

3. **A 100-MHz macropipelined VAX microprocessor**
Badeau, R.W.; Bahar, R.I.; Bernstein, D.; Biro, L.L.; Bowhill, W.J.; Brown, J.F.; Castelino, R.W.; Cooper, E.M.; Delaney, M.A.; Deverell, D.R.; Edmonson, J.H. Fischer, T.C.; Fox, T.F.; Gowan, M.K.; Gronowski, P.E.; Herrick, W.V.; Jain, A. Miner, D.G.; Partovi, H.; Peng, V.; Preston, R.P.; Somanathan, C.; Stamm, R.L Uhler, G.M.; Wade, N.D.; Wheeler, W.R.;
Solid-State Circuits, IEEE Journal of
Volume 27, Issue 11, Nov. 1992 Page(s):1585 - 1598
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Quantum Electronics, IEEE Journal of
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5. **Restructuring of first courses in power electronics and electric drives tha digital control**
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Power Electronics, IEEE Transactions on
Volume 18, Issue 1, Part 2, Jan. 2003 Page(s):429 - 437
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Vusirikala, V.; Gopalan, B.P.; Kareenahalli, S.; Merritt, S.A.; Dagenais, M.; Wo D.;
Photonics Technology Letters, IEEE
Volume 8, Issue 9, Sept. 1996 Page(s):1130 - 1132
Digital Object Identifier 10.1109/68.531812
AbstractPlus | References | Full Text: PDF(232 KB) IEEE JNL

2. **Practical approach to design and fabrication of antireflection coatings fo optical amplifiers**
Prakasam, R.; Fox, S.; Gopalan, B.P.; Kareenahalli, S.; Heim, P.J.S.; Dagenai
Photonics Technology Letters, IEEE
Volume 8, Issue 4, April 1996 Page(s):509 - 511
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5	BRS	L27	0	713/502.ccls. and (maximum adj reverse)	USPAT	2005/12/16 15:19
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